

REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-6 are presently active in this case; Claims 7-21 having been withdrawn from consideration.

In the outstanding Office Action, Claims 1-3 and 5-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fang (U.S. Pat. No. 6,023,085), Resinger (U.S. Pat. No. 6,137,718), Pradeep et al (U.S. Pat. No. 6,228,713), and Jang et al (U.S. Pat. No. 5,786,262). Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Fang, Pradeep et al, Jang et al, and Reisinger, and further in view of Agarwal et al (U.S. Pat. No. 6,201,276).

Presently active Claim 1 defines a nonvolatile semiconductor memory having a semiconductor substrate, a first transistor formed on a surface of the semiconductor substrate and including a first gate insulating film and a first gate electrode, a second transistor formed on the surface of the semiconductor substrate and including a second gate insulating film and a second gate electrode laterally separate from the first gate electrode, a trench isolating the first transistor from the second transistor, in which a bottom insulating film is formed on an inner surface of the trench and an insulating film fills the trench on the bottom insulating film, and a charge storage layer included in the first gate insulating film and absent from the second gate insulating film. The charge storage layer in the first transistor exists only below the first gate electrode in an element region, a height of the charge storage layer above the semiconductor substrate is lower than a height of the insulating film, and a width of the charge storage layer corresponds to a width of an element region of the semiconductor substrate and a thickness of the bottom insulating film.

The Office Action acknowledges that Fang do not show a first and second transistor isolated by a trench.¹ The Office Action asserts that Reisinger teaches to form an ONO gate insulating layer 5 with a silicon nitride layer 52 as a charge storage layer, and that the thickness of the bottom oxide layer 51 is smaller than the top oxide layer 53.² However, in lines 46-56 of column 5 of Reisinger, there is a description that the first oxide layer 51 has a thickness of 3 to 6 nm, and the second oxide layer 53 has a thickness of 3.5 to 6.5 nm. Therefore, it is not correct that, in Reisinger, the thickness of the bottom oxide layer 51 is smaller than the top oxide layer 53.

Furthermore, Reisinger does not show the features set forth in Claim 1 in which a trench isolates the first and second transistors, a height of a charge storage layer is lower than a height of an insulating film filling the trench on a bottom insulating film, and a width of the charge storage layer corresponds to a width of an element region of a semiconductor substrate and a thickness of a bottom insulating film.

The Office Action asserts that Pradeep et al teach to isolate memory cells with trench isolations 24 with the charge storage layer 14.³ However, according to the configuration shown in Fig. 7A of Pradeep et al, the floating gate 14 is formed lower than the top surface of the trench isolation (STI) insulating film 24, and the side surface 14A of the floating gate 14 contacts the side surface of the STI insulating film 24, directly. Hence, the configuration in Pradeep differs from the features set forth in present Claim 1.

Additionally, the Office Action asserts that Jang et al teach to form a bottom insulating layer in a trench's inner surface 10 to provide better isolation.⁴ However, this understanding of Jang et al is not correct, and the combination is improperly based on hindsight

¹ Office Action, page 3, line 10 (although Ogura et al, not applied, is cited therein).

² Office Action, page 3, lines 18-22.

³ Office Action, page 3, line 28, to page 4, line 5.

⁴ Office Action, page 4, lines 11-12.

reconstruction. Jang does not show a final configuration of a completed device. Rather, Jang et al show in Figure 10 an intermediate configuration during a STI element isolation process. Subsequently, the silicon nitride layer 6 (e.g., a charge storage layer) is removed, and does not exist in the completed device.

Moreover, the court in In re Mercier, 185 USPQ 774 (C.C.P.A. 1975) stated that

The board's approach amounts, in substance, to nothing more than a hindsight "reconstruction" of the claimed invention by relying on isolated teachings of the prior art without considering the over-all context within which those teachings are presented. Without the benefit of appellant's disclosure, a person having ordinary skill in the art would not *know what portions of the disclosure of the reference to consider and what portions to disregard as irrelevant, or misleading*. See In re Wesslau, 53 CCPA 746, 353 F.2d 238, 147 USPQ 391 (1965). [emphasis added]

Here, without knowledge of Applicant's disclosure, one would not know what portions of the disclosure of the Jang et al reference to retain and modify, and one would not know what portions to disregard as irrelevant, or misleading. Further, any adjustment in the width of the silicon nitride layer 6 in Jang et al to correspond to a width of an element region and a thickness of a bottom insulating film 14, represents impermissible hindsight reconstruction based on Applicant's disclosure. Thus, it appears that the Office Action in this case is impermissibly picking and choosing selected parts of the Jang et al reference to apply.

Hence, Applicant submits firstly that Jang et al first do not teach the features set forth in Claim 1, and secondly that the asserted combination in the Office Action is based on impermissible hindsight reconstruction and therefore improper.

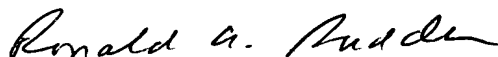
Hence, with none of the applied references singularly or in combination disclosing the features set forth in presently active Claim 1 and with the asserted combination further being improper, the present outstanding rejections should be removed, and independent Claim 1 and dependent Claims 2-6 should be allowed.

Application No. 09/955,076
Reply to Office Action of July 26, 2004

Consequently, in view of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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